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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,137	11/20/2003	Neal W. Meyer	10017494-1	9081

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EXAMINER	
THOMAS, TONIAE M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,137	MEYER ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *11-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6 and 8-10* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/718,137. Currently, claims 1-28 are pending.

Election/Restrictions

2. Applicant's election without traverse of Group I(A) (claims 1-10) in the reply filed on 28 September 2004 is acknowledged. Claims 11-17 and 23-28 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Claims 18-22 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. *Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The phrase "single-crystal silicon wafer" lacks antecedent basis (claim 5, line 2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. *Claims 1-3, 5, 8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Forbes (US 6,093,623).*

The Forbes patent discloses a method of making a multi-layered storage structure (figs. 2-9 and accompanying text). The method comprises the steps of: forming a device layer 15 on a silicon wafer 12 (fig. 2 and col. 3, lines 37-44 and lines 48-57);[1] cleaving the device layer 14 from the wafer 12 (fig. 4 and col. 4, line 65 - col. 5, line 18); repeating the forming and cleaving to provide a plurality of cleaved device layers (figs. 7, 8 and col. 6, lines 10-35); and bonding the cleaved device layers together to form the multi-layered storage structure (figs. 7, 8 and col. 6, lines 10-35).

The forming step comprises implanting devices on the wafer, as recited in claim 2 (fig. 5 and col. 5, lines 47-53).

Transistors are formed in the device layer, as recited in claim 3 (figs. 5, 6, col. 5, lines 47-53, and col. 6, lines 1-9).

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[1] Presumably the silicon is single crystal silicon, since Forbes does not state otherwise.

The step of repeating comprises forming the plurality of cleaved device layers from the same single-crystal silicon wafer 12, as recited in claim 5 (fig. 7 and col. 6, lines 10-25).

In one embodiment, the cleaving comprises ion-implantation induced layer splitting of the wafer, as recited in claim 8 (col. 5, lines 9-18).

The storage structure comprises memory or a processor, as recited in claim 10 (fig. 9 and col. 6, lines 40-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. *Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes in view of Farrens et al. (US 6,180,496 B1).*

Forbes does not teach that the bonding of device layer 29 to the cleaved device layer as shown in figure 7 comprises plasma-activated bonding, as recited in claim 6. The Farrens et al. patent (Farrens) discloses a method for bonding semiconductor wafers and other materials to one another using an in situ plasma wafer bonding method (col. 5, lines 4-62). The method comprises: placing wafers in a plasma chamber equipped with bonding apparatus; exposing the wafers to a plasma; and without breaking vacuum, placing the

wafer surfaces together, thereby bonding the substrates together (col. 5, lines 38-43). The resulting bonded materials are free from macroscopic and microscopic voids, and the initial bond is much stronger than conventional bonding techniques (abstract, lines 9-13).

Since both the Forbes and Farrens patents are from the same field of endeavor, the purpose for which Farrens is relied upon would have been recognized in the pertinent reference of Forbes by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Forbes by bonding the device layer to the cleaved device layer using a plasma-activated bonding method, as taught by Farrens, for the following reasons: the initial bond formed between the two layers when a plasma-activated bonding method is used is much stronger than the bond resulting from conventional bonding techniques; and the layers that are bonded together using a plasma-activated bonding method are free from macroscopic and microscopic voids.

6. *Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes in view of Usenko (US 6,352,909).*

Forbes does not teach that the cleaving comprises anodic etching and annealing of the wafer, as recited in claim 9. Usenko discloses a method for cleaving a single crystal silicon wafer (figs. 2A-2G and col. 3, line 41 - col. 4, line 27). The cleaving method comprises an anodic etching of the single crystal

wafer 1 (fig. 2D and col. 3, line 66 - col. 4, line 5), and a subsequent annealing of the wafer (figs. 2F, 2G, and col. 4, lines 17-27).

Since both the Forbes and Usenko patents are from the same field of endeavor, the purpose for which Usenko is relied upon would have been recognized in the pertinent reference of Forbes by one of ordinary skill in the art at the time the invention was made.

As explained above, Forbes discloses cleaving the device layer using ion-implantation induced layer splitting of the wafer. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Forbes by cleaving the device layer from the wafer using anodic etching and annealing, as taught by Usenko, since anodic etching and annealing is an alternate cleaving method that may be used in place of ion-implantation induced layer splitting of the wafer.

Allowable Subject Matter

7. *Claims 4 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.* The prior art of record does not anticipate, teach or suggest a method of making a multi-layered storage structure substantially as claimed, wherein the device layer comprises vertical diodes and the storage structure is a vertical memory structure, as recited in claim 4, or wherein the bonded device layers form a three-dimensional cross-point array memory structure, as recited in claim 7.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
09 December 2004

Mary Wilczewski
Primary Examiner